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Claims

[c1] 1. A method for forming a PN junction, comprising:
forming a stacked structure on a substrate, wherein the stacked structure comprises, from bottom to top, a first doped layer, a dielectric layer and a nucleation layer;
forming an insulating layer over the substrate, the insulating layer having an opening therein exposing a portion of the nucleation layer;
forming a second doped layer of polysilicon or amorphous silicon in the opening;
performing an annealing process to convert the second doped layer into a first single-crystal silicon layer; and
breaking down the dielectric layer, wherein
one of the first doped layer and the second doped layer is P-doped, and the other is N-doped.

[c2] 2. The method of claim 1, wherein the first doped layer comprises a second single-crystal silicon layer.

[c3] 3. The method of claim 1, wherein the first doped layer comprises a polysilicon layer.

[c4] 4. The method of claim 3, wherein a major carrier concentration of the second doped layer is lower than a ma-

jor carrier concentration of the first doped layer.

[c5] 5. The method of claim 1, wherein the nucleation layer comprises a silicon nitride layer.

[c6] 6. A method for forming a PN junction, comprising:
forming a stacked structure on a substrate, wherein the stacked structure comprises, from bottom to top, a first doped layer, a dielectric layer and a second doped layer of polysilicon or amorphous silicon, wherein one of the first doped layer and the second doped layer is P-doped, and the other is N-doped;
forming an insulating layer over the substrate, the insulating layer having an opening therein exposing a portion of the second doped layer;
forming a nucleation layer on the second doped layer exposed by the opening;
performing an annealing process to convert the portion of the second doped layer under the nucleation layer into a first single-crystal silicon layer; and
breaking down the dielectric layer.

[c7] 7. The method of claim 6, wherein the first doped layer comprises a second single-crystal silicon layer.

[c8] 8. The method of claim 6, wherein the first doped layer comprises a polysilicon layer.

[c9] 9. The method of claim 8, wherein a major carrier concentration of the second doped layer is lower than a major carrier concentration of the first doped layer.

[c10] 10. The method of claim 6, wherein forming the nucleation layer comprises forming a germanium (Ge) seed layer.

[c11] 11. A one-time programmable read-only memory (OTP-ROM) process, comprising:
(a) providing a substrate having an insulating layer and linear stacked structures formed thereon, wherein the linear stacked structures are embedded in trenches of the insulating layer, and each linear stacked layer includes, from bottom to top, a semiconductor layer of a first conductivity type, an anti-fuse layer and a nucleation layer;
(b) forming a next insulating layer over the substrate;
(c) forming a plurality of trenches in the next insulating layer in an orientation different from an orientation of the trenches in the former insulating layer, so that multi-portions of each nucleation layer are exposed;
(d) filling a polysilicon layer of a second conductivity type into each trench in the next insulating layer; and
(e) performing an annealing process to convert portions of the polysilicon layers on the nucleation layers into

single-crystal silicon layers, wherein
a single-crystal silicon layer, the nucleation layer and the antifuse layer under the single-crystal silicon layer, and a portion of a semiconductor layer under the single-crystal silicon layer together constitute a memory cell.

[c12] 12. The OTP-ROM process of claim 11, wherein each linear stacked structure further comprises a conductive layer under the semiconductor layer; and
the OTP-ROM process further comprises:
(f) filling a next conductive layer in each trench of the next insulating layer.

[c13] 13. The OTP-ROM process of claim 12, further comprising the following steps for forming a 3D memory:
(g) forming a next semiconductor layer, a next antifuse layer and a next nucleation layer on the conductive layer in each trench of the next insulating layer, so as to form a next stacked structure; and
cyclically repeating the steps (b)-(g) to form upper insulating layers and linear stacked structures until a predetermined number of layers of memory cells are fabricated, wherein the orientation of the trenches formed in one insulating layer is different from that of the trenches formed in an adjacent insulating layer, and the step (g) is not performed in the last cycle of steps.

[c14] 14. The OTP-ROM process of claim 11, wherein the nucleation layer comprises a silicon nitride layer.

[c15] 15. A one-time programmable read-only memory (OTP-ROM) process, comprising:
(a) providing a substrate having an insulating layer and linear stacked structures formed thereon, wherein the linear stacked structures are embedded in trenches of the insulating layer, and each linear stacked layer includes, from bottom to top, a semiconductor layer of a first conductivity type, an antifuse layer and an amorphous silicon layer of a second conductivity type;
(b) forming a next insulating layer over the substrate;
(c) forming a plurality of trenches in the next insulating layer in an orientation different from an orientation of the trenches in the former insulating layer, so that multi-portions of each amorphous silicon layer in the former insulating layer are exposed;
(d) forming a nucleation layer in each trench of the next insulating layer;
(e) performing an annealing process to convert the portions of the amorphous silicon layers under the nucleation layers into single-crystal silicon layers;
(f) removing the nucleation layers; and
(g) forming a conductive layer in each trench of the next insulating layer, wherein

a single-crystal silicon layer, the antifuse layer under the single-crystal silicon layer and a portion of a semiconductor layer under the single-crystal silicon layer together constitute a memory cell.

[c16] 16. The OTP-ROM process of claim 15, wherein forming the nucleation layers in the trenches of the next insulating layer comprises:
selectively depositing germanium on the portions of the amorphous silicon layers exposed by the trenches of the next insulating layer; and
performing an annealing process to convert the deposited germanium into single-crystal germanium.

[c17] 17. The OTP-ROM process of claim 15, further comprising:
(h) forming a next semiconductor layer of the first conductivity type and a next antifuse layer on the conductive layer in each trench of the next insulating layer;
(i) forming a next amorphous silicon layer of the second conductivity type over the substrate;
(j) forming a plurality of linear nucleation layers on the next amorphous silicon layer, wherein each linear nucleation layer is located over a next semiconductor layer;
(k) performing an annealing process to convert the portions of the next amorphous silicon layer under the linear nucleation layers into single-crystal silicon layers;

(l) removing the linear nucleation layers;

(m) forming a next conductive layer on the next amorphous silicon layer including the single-crystal silicon layers; and

(n) patterning the next conductive layer and the next amorphous silicon layer including the single-crystal silicon layers to form a plurality of linear stacked structures that have an orientation different from an orientation of the trenches in the next insulating layer.

[c18] 18. The OTP-ROM process of claim 17, wherein the step (j) of forming a plurality of linear nucleation layers on the next amorphous silicon layer comprises:

forming a mask layer on the next amorphous silicon layer;

patterning the mask layer to form a plurality of trenches, wherein each trench exposes a linear portion of the next amorphous silicon layer that overlies a next semiconductor layer; and

selectively forming single-crystal germanium on the linear portions of the next amorphous silicon layer to serve as the nucleation layers; and

the OTP-ROM process further comprising:

removing the mask layer before the next conductive layer is formed.

[c19] 19. The OTP-ROM process of claim 17, wherein the step (m) further comprises sequentially forming a still next semiconductor layer of the first conductivity type, a still next antifuse layer and a still next amorphous silicon layer of the second conductivity type; and the step (n) comprises patterning the still next amorphous silicon layer, the still next antifuse layer, the still next semiconductor layer, the next conductive layer and the next amorphous silicon layer to form a plurality of linear stacked structures that have an orientation different from an orientation of the trenches in the next insulating layer; and

the OTP-ROM process further comprises:

(o) filling a still next insulating layer in between the linear stacked structures formed in the step (n); and

cyclically repeating the steps (b)-(o) to form higher insulating layers and linear stacked structures until a predetermined number of layers of memory cells are fabricated, wherein the OTP-ROM process is terminated on a step (g) or a step (n), and when the OTP-ROM process is terminated on a step (n), the terminal step (n) and the step (m) just before the terminal step (n) are according to claim 21.

[c20] 20. A one-time programmable read-only memory (OTP-ROM) cell, comprising:

a first doped layer of a first conductivity type on a substrate;
an antifuse layer on the first doped layer;
a nucleation layer on the antifuse layer; and
a second doped layer of a second conductivity type on the nucleation layer, wherein a material of the second doped layer is single-crystal silicon.

[c21] 21. The OTP-ROM cell of claim 20, wherein the first doped layer comprises a single-crystal silicon layer.

[c22] 22. The OTP-ROM cell of claim 20, wherein the first doped layer comprises a polysilicon layer.

[c23] 23. The OTP-ROM cell of claim 22, wherein a major carrier concentration of the second doped layer is lower than a major carrier concentration of the first doped layer.

[c24] 24. The OTP-ROM cell of claim 20, wherein the nucleation layer comprises a silicon nitride layer.

[c25] 25. A one-time programmable read-only memory (OTP-ROM) device, comprising:
a plurality of linear stacked structures, wherein each linear stacked structure comprises, from bottom to top, a semiconductor layer of a first conductivity type, an antifuse layer and a nucleation layer; and

a plurality of linear silicon layers of a second conductivity type crossing over the linear stacked structures, wherein each linear silicon layer comprises a plurality of polysilicon blocks and single-crystal silicon blocks that are arranged alternately, wherein a single-crystal silicon block is on the nucleation layer of a linear stacked structure that overlaps with the linear silicon layer, and a polysilicon block is between two single-crystal silicon blocks.

[c26] 26. The OTP-ROM device of claim 25, wherein each linear stacked structure further comprises a bottom conductive layer under the conductive layer, and each linear silicon layer is disposed with an upper conductive layer thereon.

[c27] 27. The OTP-ROM device of claim 25, wherein the nucleation layer comprises a silicon nitride layer.

[c28] 28. A one-time programmable read-only memory (OTP-ROM) device, comprising:
at least three layers of linear stacked structures, wherein each layer includes a plurality of linear stacked structures, and an orientation of the linear stacked structures of one layer is different from an orientation of the linear stacked structures of an adjacent layer, wherein
each linear stacked structure comprises, from bottom to top, a silicon layer of a second conductivity type, a con-

ductive layer, a semiconductor layer of a first conductivity type, an antifuse layer and a nucleation layer;

each linear stacked structure of the lowest layer does not include a silicon layer of the second conductivity type, and each linear stacked structure of the highest layer does not include a semiconductor layer of the first conductivity type, an antifuse layer and a nucleation layer; and

each silicon layer of the second conductivity type includes a plurality of single-crystal silicon blocks and a plurality of polysilicon blocks that are arranged alternately, wherein a single-crystal silicon block is on the nucleation layer of a lower linear stacked structure that overlaps with the silicon layer, and each polysilicon block is between two single-crystal silicon blocks.

[c29] 29. A one-time programmable read-only memory (OTP-ROM) device, comprising:

a plurality of linear stacked structures on a substrate, wherein each linear stacked structure includes, from bottom to top, a semiconductor layer of a first conductivity type, an antifuse layer and a silicon layer of a second conductivity type; and

a plurality of linear conductive layers crossing over the linear stacked structures, wherein

each silicon layer of the second conductivity type com-

prises a plurality of amorphous silicon blocks and a plurality of single-crystal silicon blocks that are arranged alternately, wherein a single-crystal silicon block is under a linear conductive layer that overlaps with the silicon layer, and an amorphous silicon block is between two single-crystal silicon blocks.

[c30] 30. A one-time programmable read-only memory (OTP-ROM) device, comprising:
at least three layers of linear stacked structures, wherein each layer includes a plurality of linear stacked structures, and an orientation of the linear stacked structures of one layer is different from an orientation of the linear stacked structures of an adjacent layer, wherein
each linear stacked structure in an odd layer comprises, from bottom to top, a lower silicon layer of a second conductivity type, a conductive layer, a semiconductor layer of a first conductivity type, an antifuse layer and an upper silicon layer of the second conductivity type, wherein each linear stacked structure of the first/lowest layer does not include a lower silicon layer, and when the highest layer is an odd layer, each linear stacked structure of the highest odd layer does not include an semiconductor layer of the first conductivity type, an antifuse layer and an upper silicon layer;
each linear stacked structure in an even layer comprises,

from bottom to top, a conductive layer, a semiconductor layer of the first conductivity type and an antifuse layer, and when the highest layer is an even layer, each linear stacked structure of the highest even layer does not include a semiconductor layer and an antifuse layer;

each lower silicon layer of an odd layer comprises a plurality of lower single-crystal silicon blocks and a plurality of lower amorphous silicon blocks that are arranged alternately, wherein a lower single-crystal silicon block is located on the antifuse layer of a lower linear stacked structure that overlaps with the lower silicon layer, and each lower amorphous silicon block is between two lower single-crystal silicon blocks; and

each upper silicon layer of an odd layer comprises a plurality of upper single-crystal silicon blocks and a plurality of upper amorphous silicon blocks that are arranged alternately, wherein an upper single-crystal silicon block is under the conductive layer of an upper linear stacked structure that overlaps with the upper silicon layer, and each upper amorphous silicon block is between two upper single-crystal silicon blocks.